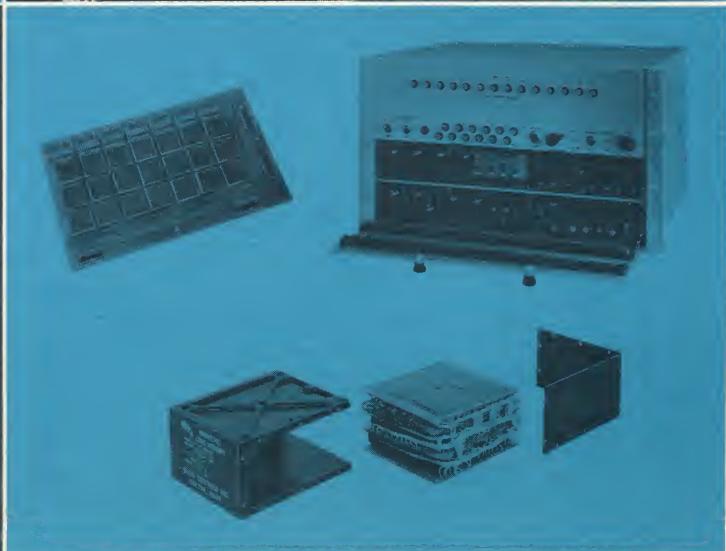
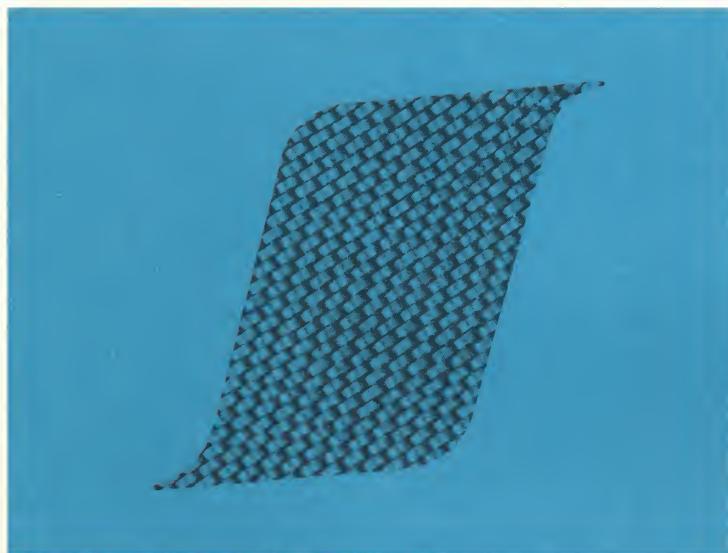




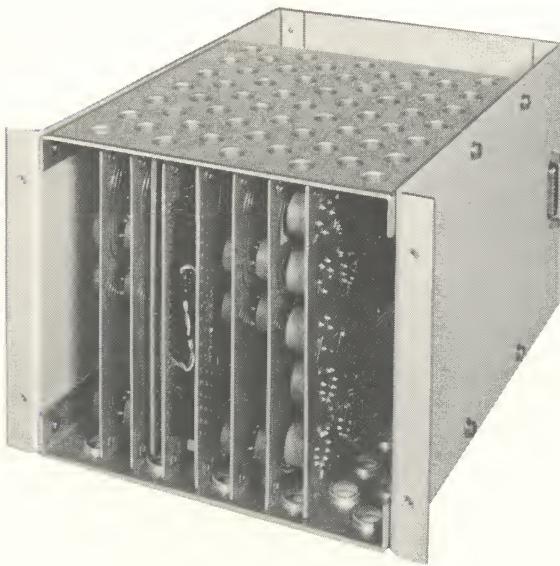
DI/AN CONTROLS, INC. 944 DORCHESTER AVENUE, BOSTON, MASSACHUSETTS 02125
Telephone (617) 288 7700, TWX 710-333-0174

MAGNETIC CORE MEMORY SYSTEMS

DI/AN CONTROLS manufactures Serial, Sequential and Random Access magnetic core memory systems. They are designed for inclusion in Aerospace, Airborne, Military and Commercial environments. These systems provide the widest **flexibility in size, capacity, weight, speed, configuration, environmental specifications, and options**. During the past decade, DI/AN has designed and delivered more severe environment memory systems than any other supplier. The design staff includes several of the leading pioneers in memory techniques and innovation. Production facilities are integrated and advanced; management is program oriented. Quality control, quality assurance and documentation procedures are in accordance with the most stringent governmental standards. Severe environmental testing is an in-house capability.



The MCDL-50 is a BIT SERIAL CORE MEMORY SYSTEM for **economical data formatting and limited capacity storage**. This "off-the-shelf" buffer system meets applications previously filled by more expensive, less reliable multiple delay lines. The MCDL series features speeds up to 20 μ s, non-volatile data storage, low standby-power, high noise-immunity, high storage-density, modular construction and all silicon circuitry. Four models are available providing a full range of operating modes.



MCDL - 50 SERIES BUFFER

OPERATING CHARACTERISTICS

Bit Rate	0 to 5×10^4 Bits/Sec (asynchronous)
Storage Capacity	Up to 1386 Bits
Operating Modes	Read/Restore; Clear/Write
Input Data	Bit Serial or up to 12 Parallel Bits
Output Data	Bit Serial or up to 16 Parallel Bits
Voltage Requirements	-6, +6, +28 volts

APPLICATIONS (Four Models Available)*

Communications Terminal Buffer	
Transmitter	MCDL-P/S
Receiver	MCDL-S/P
Data Formatting	
Serial-Parallel	MCDL-S/P
Parallel-Serial	MCDL-P/S
n Parallel —	
m Parallel	MCDL-P/P
Block or Line Buffer	MCDL-S/S
I/O Buffer	MCDL-P/P
Event Indexer	MCDL-S/S
Telemetering Buffer	MCDL-S/P MCDL-P/S

* MCDL-S/S Bit Serial In; Bit Serial Out

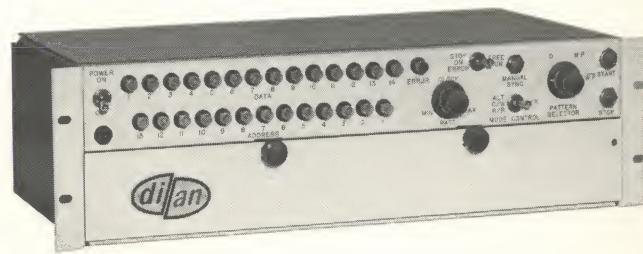
MCDL-S/P Bit Serial In; Bit Parallel Out

MCDL-P/S Character Parallel In; Bit Serial Out

MCDL-P/P Character Parallel In; Character Parallel Out

For further information write for Bulletin 3-300

A highly reliable Sequential Access Buffer, the **DI/AN SA Series**, employs internally-addressed, coincident-current, magnetic core memories for a **wide variety of data buffering applications**. Two basic models are available: The SA-1A and the SA-VB. The SA-1A is a basic sequential buffer employing one address counter and operates in load/unload sequence at each address in turn. The SA-VB is a fully interlaced buffer having two address registers which permit load/unload operations to be interlaced in turn. Both systems achieve **high reliability** through the use of one **low component-count potted drive circuit type** that performs address storage and decoding, supplies core drive current and advances the address. The SA Series operating rate of 100 KC fulfills the majority of applications, however, faster unit speeds are available upon request.



SA SERIES BUFFER

MEMORY SPECIFICATIONS

Full Cycle Time SA-1A	10 μ sec
SA-VB	10 μ sec
Load Rate for VB-200	5 μ sec
VB-100	10 μ sec
Unload Rate	Same as above
Storage Capacity: Words	36, 72, 144, 240, 336, 540, 756, 1056
Bits	4, 6, 8, 10, 12
Access Modes	Sequential, sequential interlaced
Operating Modes	Load — Unload
Interface Voltage Levels	0 to -6v; others available on request
Temperature	0°C to +50°C
Physical Dimension	19" EIA, rack mounted. A typical 336 word x 6 bit unit including power supply is 3½ inches high.

For further information write for Bulletin 61-40

ABOUT DI/AN CONTROLS/FACILITIES, CAPABILITIES.

Historical Note

At **DI/AN** major research efforts in magnetic memory design have their roots in the original work on magnetic drums, tapes and recording media done at Harvard University as early as 1946-47, and in the basic studies conducted from 1951 through 1954 on magnetic materials, circuits and logical structures.

The years 1954 to 1958 produced solutions to problems introduced by large scale manufacturing . . . problems involving material uniformity, economical production techniques, and the need for operating margins in severe environments.

The reservoir of skills developed at **DI/AN** since 1958 encompass basic research, product design and development, manufacturing methods, systems application, program management, reliability and quality control. These skills are continually applied to new proprietary products in the broad field of digital magnetics.

The following successful firsts in magnetic core memories and related fields are credited to **DI/AN** — the only organization **specializing wholly** in digital magnetics.

- Digital Magnetic Drum — 1946-47
- Magnetic Digital Logic — 1951
- One-Core-Per-Bit Magnetic Shift Registers — 1952
- Core-Transistor Logic Elements — 1953
- Magnetically Addressed Core Memories — 1954
- Wide Temperature Range Coincident-Current Core Memories — 1955
- Solid State Aerospace Digital Computer — 1954-55
- Sub-Microsecond Core Memory — 1961

Established Memory Products

As a natural outgrowth of its research and development efforts, **DI/AN** is fully committed to well established production activities in two major memory areas: (1) NASA and DOD qualified aerospace miniature memories, and (2) commercial coincident-current buffer storage units, both sequential and random access. Both product groups have grown in parallel — that is, one is not an off-shoot of the other, but rather an interdependence of ideas and approaches has always existed in every critical implementation phase. As a consequence of this, **DI/AN's** commercial memory series enjoys, for example, the same high quality level as its counterparts in aerospace equipments; there is no question that both have gained the

benefits of **DI/AN** advanced technology in the key areas of circuit design, system optimization, and manufacturing approach.

Applied Research in System Integration

Not limited to strictly OEM procurements of its memory products, **DI/AN** has also developed several large electromechanical system product lines employing its own "home-grown" memory systems; notable among these are (1) high-speed computer-interfaced line printers, and (2) Computer Keyboard, a computerized typesetting system for supplying newspaper linecasting machines with clean, justified punched paper tape. In addition, **DI/AN** developed (in 1962) the data manipulator and control system electronics presently employed in the MEDLARS-GRACE photocomposing typesetter system in use at the National Library of Medicine. **DI/AN** welcomes projects calling for the integration of memory techniques with OEM products as well as industrial systems and documentation procedures.

Manufacturing

DI/AN maintains two shifts in its memory system manufacturing department. All of **DI/AN's** working facilities are fully outfitted with advanced equipment providing a performance capability which can readily meet the most demanding state-of-the-art requirements for digital magnetic systems and components.

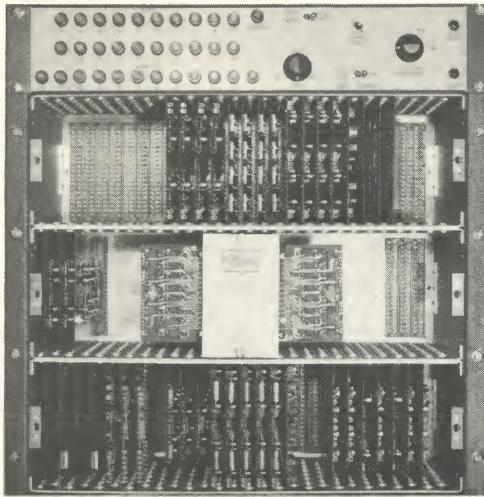
Quality Assurance

At **DI/AN** reliability is designed into its memory products. And because each worker has a strong awareness of the vital nature of his job as well as the end products, this reliability is never lost in production. The **DI/AN** concept of control may be summarized as follows: setting standards for cost performance and quality, establishing procedures and designing the system to guide the quality effort; appraising conformance, and taking corrective measures. QC and reliability efforts are based upon the following specifications: NPC-200 (2, 3, 4), MIL Q 9858A, NPC-250-1, MIL R-27542.

Research & Development

DI/AN has demonstrated repeatedly its capacity for timely delivery of reliable equipment and systems meeting unusual and stringent specifications. Behind this capacity are men of broad technical scope, with a well documented history of invention in the areas of digital magnetic circuitry and advanced data storage, processing and control systems. This sophistication is reflected in each and every memory system **DI/AN** has ever produced.

Military and commercial applications requiring economical high-speed random access operation are supplied by the RSA-STD-500 and RSA-MIL-500 **high-speed, integrated circuit magnetic core memory family**. Full cycle time is 2 microseconds. Both models feature a high degree of modularity employing both plug-in memory stacks and component cards for easy maintenance. Silicon semiconductor circuitry and core configurations designed for wide temperature operations make up the remaining electronics. User can increase storage capacity in the field.



RSA SERIES MEMORY

MEMORY SPECIFICATIONS

Full Cycle Time	2 microseconds
Access Time	800 nanoseconds
Storage Capacity	64 to 4096 words. Expandable in 4096 blocks to 32,768 4-28 bits/word modularly expandable to 64 bits/word
Access Modes	Random Sequential Random/Sequential Sequential Interlaced
Operating Modes	Read/Restore Clear/Write Read/Modify/Write (2 μ sec) Read/Modify/Write (extended cycle)
Interface Levels	TTL Integrated Circuitry
Physical Specifications	19-inch EIA rack mounted
Environmental Specifications	
Operating Temperature	+10 to +45°C 0 to +80°C (MIL)
Relative Humidity	Up to 90%
Shock	15 G's std. com.

For further information write for Bulletin 3-200

MISSION PROVEN MEMORY AIRBORNE AND DEEP SUBM

The history of aerospace accomplishments in the field of memory systems attests to the fact that **DI/AN CONTROLS** has supplied a wide range of memory products in greater numbers, for more government programs, over a longer period of time than any other manufacturer. Re-orders for these equipments, time and again, prove their high performance, reliability and cost feasibility. Complete program

MRA-100 and MRA-250 MINIATURE RAND

DI/AN's MRA-100 and MRA-250 are Miniature Random Access Memory Units, developed primarily for aerospace and airborne applications where high speed, reliability, low weight, low power and volume are the prime criteria. Both the "100" and "250" systems are operationally identical and differ only in operating rate and physical size.

Specifications:

Storage	256 to 4096 words 2 to 28 bits/word
Operating Rate	0 to 250 KHz 0 to 100 KHz
Cycle Time (C/W or R/R):	4 μ sec*; 10 μ sec *slight increase in volume
Access Time	1.0 μ sec max.
Dimensions	5 $\frac{1}{2}$ " x 7" x H where H varies from 3" to 6" depending on total storage capacity and operating rate.
Weight	6 lbs. max. for largest capacity system
Storage Temperature:	-65°C to +125°C

For further information write for Bulletin 3-600

MSA-80 MINIATURE SEQUENTIAL ACCESS AER

The Miniature Memory, Model MSA-80 Buffer Storage is a miniature, sequential access, coincident current core memory with internal addressing. It is small, light, compact, rugged and meets all necessary environmental and shock specifications for Aero Space Applications. Magnetic Core Circuits are used for all control, addressing, writing and reading functions, thus keeping the semiconductor count low and reliability high. All circuit components and memory cores are completely encapsulated in special epoxy compounds. Data input and output is asynchronous and can proceed at any rate up to rated maximums. This series is characterized by extremely low power consumption and data retention without power (non-volatile store), even in the maximum capacity memory. Standard in this series are 12 different word capacities ranging from 210 to 10,296 words, with one to ten bits per word. Other combinations are available with minor design and production changes.

Specifications:

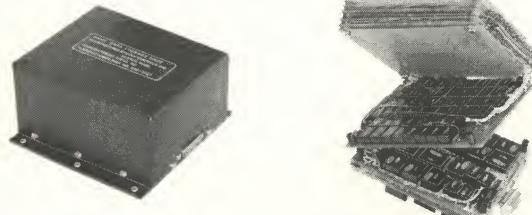
Storage	Up to 102,960 bits
Operating Rate	0 to 80 KHz
Load/Unload Rate	Full cycle; 12.5 μ sec
Access Time	4.5 μ sec max.
Volume	Form factor 4:3:1
Weight	Dependent upon capacity. Typical: 30,000 bits less than 4 lbs.
Storage Temperature	-65°C to +125°C
Operating Temperature	-55°C to +100°C -30°C to +65°C

For further information write for Bulletin 3-500

SYSTEMS FOR AEROSPACE, EMERGENCY APPLICATIONS

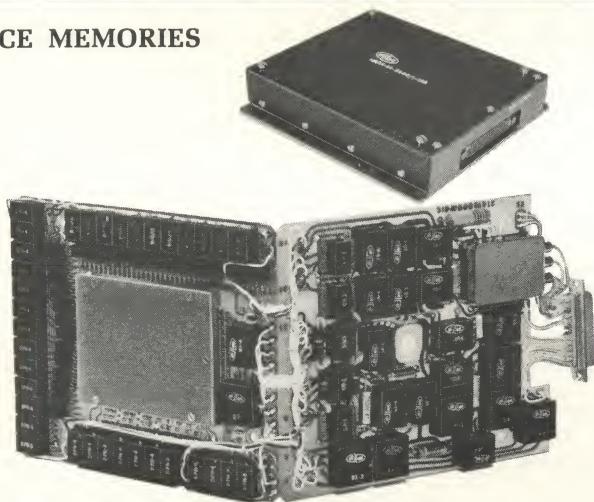
management capability is the key to this performance. Should requirements exist for memories that fall within the standard ranges, **DI/AN** will be pleased to quote delivery and price immediately. Where more advanced specifications are required, the engineering staff is prepared to study the problem and submit a proposal. The products shown are typical of **DI/AN** aerospace competence.

ROM ACCESS AEROSPACE MEMORIES



Operating Temperature	-55°C to +100°C -30°C to +65°C
Input Signal Levels	Binary 0 = 0 to +0.9v Binary 1 = +3 to +5.5v
Output Signal Levels	Binary 0 = +0.4v max. Binary 1 = +3.0v min.
Voltage Requirement	+12, +5, -6 VDC Note: >+12v necessary for the large storage capacities.
Power Requirement	Dependent upon capacity

DSPACE MEMORIES



Input Signal Levels .	Binary 0 = 0 to +1.0v Binary 1 = +3.5 to +6.0v
Output Signal Levels	Binary 0 = 0 to +0.5v Binary 1 = +3.5 to +6.0v
Voltage Requirement	+24 to +28 VDC and the one required low level logic voltage
Power Requirement	Standby; typically less than 50mw. Operating; dependent upon operating rate. Typically 100 mw per KC.

DI/AN has supplied memory systems, related equipment and engineering services for each of the major governmental programs listed. The projects span the entire breadth of environments — from beneath the ocean to those in space. These equipments have never failed in operation — an outstanding record considering that more than 600 systems are now in service.

Equipment Program Agency

AEROSPACE

Miniature Memories	Bio-Satellite AOOSO Pegasus Transit (Classified Payloads)	NASA NASA NASA USN DOD
Related Equipment	Mariner-B Discoverer SNAP Series NASA-S Series Anna Staff X-15 Agena-D Scout	NASA USAF AEC NASA NASA USAF NASA-DOD USAF NASA
System Design Consultation	Mariner-B Discoverer Pegasus Nimbus	NASA USAF NASA NASA

GROUND BASED

SA Buffers	Telstar Discoverer Mariner Surveyor U-2 Start Ariadne (Commercial)	Bell Tel. Labs USAF NASA NASA DOD USAF USAF General Dynamics Corp.
RA Buffers	Nike (Telemetry Computer) (Commercial)	DOD NASA Standard Radio Co. (Sweden)

HYDROSPACE

SA Memories	Polaris	USN
RA Memories	(Oceanographic)	USN

The systems listed above meet applicable portions of a wide variety of NASA and MIL specifications including:

MIL-E-8189	MIL-I-26600
MIL-E-4158	MIL-Q-9858
MIL-E-16400	MIL-T-55110
MIL-E-5400	MIL-STD-275
MSFC-STD-154	MSFC-PROC-158B
NPC-200 (2,3,4)	NPC-250-1

plied memory systems, related engineering services for each of mental programs listed. The project breadth of environments — ocean to those in space. These never failed in operation — and considering that more than 600 in service.

Program Agency

AEROSPACE

io-Satellite NASA
OSO NASA
egabus NASA
transit USN
Classified
ayloads) DOD
Mariner-B
iscoverer NASA
NAP Series USAF
ASA-S Series AEC
nna NASA
taff USAF
-15 NASA-DOD
gena-D USAF
cout NASA
Mariner-B
iscoverer NASA
egabus NASA
imbus NASA

GROUND BASED

elstar Bell Tel. Labs
iscoverer USAF
Mariner NASA
urveyor NASA
-2 DOD
start USAF
riadne USAF
Commercial) General Dynamics Corp.
ike DOD
Telemetry NASA
omputer) Standard Radio
ommercial) Co. (Sweden)

HYDROSPACE

Polaris USN
(Oceanographic) USN

d above meet applicable portions
of NASA and MIL specifications

MIL-I-26600
MIL-Q-9858
MIL-T-55110
MIL-STD-275
MSFC-PROC-158B
NPC-250-1

Won't you help us to help you? Should you presently have a requirement or be contemplating a need for memory systems, the DI/AN staff will be pleased to study your requirement and submit detailed technical suggestions, price and delivery quotations.

REQUIREMENTS: My application is:

- Aerospace Commercial
 Airborne Hydrospace
 Ground Based (Mobile)

The Model most closely representing my need is listed in the catalog as:

Additional features I require, (e.g., NDRO operation, address and data register display, self-tester).

FOLD AND STAPLE BEFORE MAILING

SPECIFICATIONS

Address Access: Random only
Sequential only ; both
Storage Capacity: Number of words _____
Word length _____.
Full Cycle Time: _____ μsec.
Access Time: _____ μsec.
Mechanical Size: L _____ W _____ H _____.
Applicable MIL Spec (if any) _____.
Weight: specify if important _____.
Operating Temperature _____ to _____ °C.
Shock: specify amplitude _____ period _____.
Vibration: specify amplitude _____ period _____.
Power: supplied by DI/AN ; customer
Interface Levels: input _____ output _____.

STATUS OF PROJECT

- For Information Only
 Study Stage
 Proposal Stage
 Production Stage

Name _____

Title _____

Company _____

Address _____

City _____ State _____

Zip _____ Tel. _____

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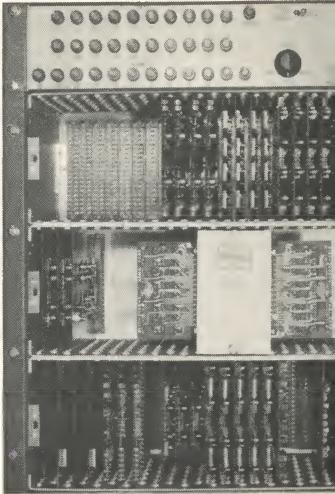
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DI/AN CONTROLS, INC.
944 DORCHESTER AVENUE
BOSTON, MASSACHUSETTS 02125

DI/AN maintains engineering and service representation in all major cities throughout the nation and in key centers overseas. These men are prepared to help you choose the most appropriate products for your needs, as well as aid in the design of special systems.

Please write to our offices for the local representative closest to your facility.

Military and commercial applications requiring economical high-speed operation are supplied by RSA-STD-500 and RSA-M series, speed, integrated circuit memory family. Full cycle time is less than one second. Both models feature a high degree of modularity employing standard memory stacks and components for easy maintenance. Silicon gate technology and core configuration provide for wide temperature operation and the remaining electronics. Increase storage capacity in the



RSA SERIES MEMORY

MEMORY SPECIFICATIONS

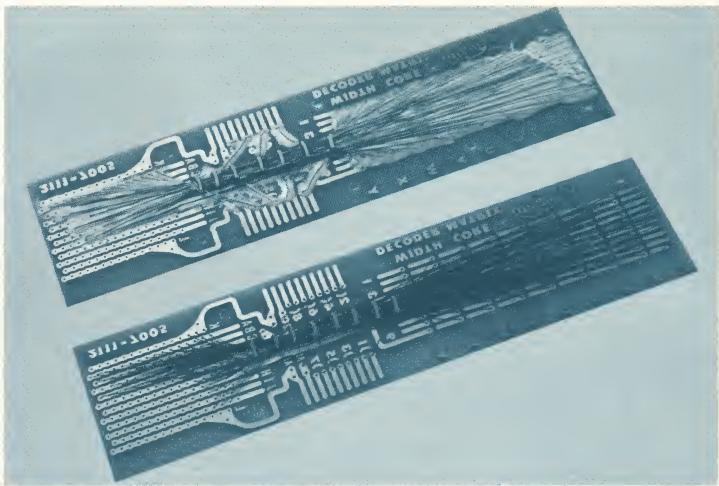
Full Cycle Time	2 microseconds
Access Time	800 nanoseconds
Storage Capacity	64 to 4096 words per block to 32,768 words 4-28 bits/word to 64 bits/word
Access Modes	Random Sequential Random/Sequential Sequential Interleaved
Operating Modes	Read/Restore Clear/Write Read/Modify/Write Read/Modify/Write TTL Integrated
Interface Levels	19-inch EIA rate
Physical Specifications	
Environmental Specifications	
Operating Temperature	
Relative Humidity	
Shock	

For further information write for Bulletin

CORE MEMORY PLANES

DI/AN designs and manufactures its own proprietary core memory planes and stacks for application in its own products ranging from low-cost commercial memories to those required to meet the special extremes of military and aerospace environments.

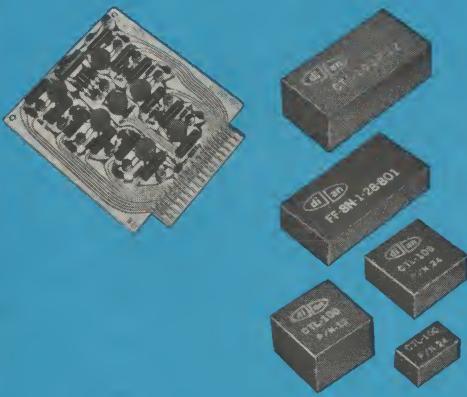
Arrays and stacks are not normally supplied to customers as a separate product, but we will be pleased to aid in the design and production of special arrays or for those calling for meaningful innovation.



OTHER DI/AN PRODUCTS

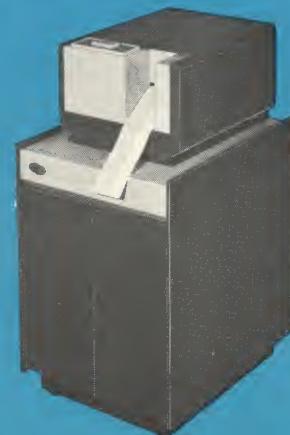
Digital-Magnetic Components Division

Specializing in digital magnetics, this Division has developed magnetic core logic modules, component cards and systems designed to operate within the stringent specifications and functional requirements of NASA and DOD. These products have a proven record of reliable performance in a variety of aerospace data processing and control applications.



Lister/Printer Products Division

This Division specializes in the design, development and manufacture of high-speed digital printing equipment capable of handling numeric and alphanumeric information for data logging, listing, addressing, labeling and data acquisition applications. In addition, complete computer interfaced printers are available for use directly with the PDP-8, SDS-92, DDP-116, H-20, Data 620 and others.



Computer Keyboard Division

This Division designs and manufactures a line of specialized typesetting equipment based on computer technology for newspapers, commercial printing and book-publishing houses.



For information on Divisional products, write for appropriate Brochures.